REMARKS/ARGUMENTS

Status of the Application

Claims 1, 5-9, 12-15, 18, 20-21 and 23-26 are pending in this application. Claims 1, 5-9 and 13 are rejected under 35 USC § 102(b). Claims 12, 14-15, 18, 20-21 and 23-26 are rejected under 35 USC § 103(a).

Rejection under 35 USC § 102(b)

Independent claims 1 and 9 are rejected as being anticipated by US Patent 3,931,613 (Gruner et al.). Applicants respectfully disagree.

As discussed in the previous response dated Dec 12, 2006, Gruner et al. describes a data processing system which includes a single memory system shared by four processors. See Gruner et al., Fig. 11 (elements 10, 11, 12, 13 and 14). The processors are grouped into first and second pair groups. The groups access the memory at different time frames. See Gruner et al., Fig. 12 and col. 12 at lines 47-51. Therefore, within the time frame allocated to a group, only one processor within that group can access the memory. Furthermore, within each time frame, only one processor can access the memory at a time. In fact, the memory system of Gruner et al. cannot support access by more than one processor at any one time since there is only a single address bus and memory data bus. See Gruner et al., Fig. 11 (elements 16 and 17). This appears to be also supported by the Examiner, acknowledging that Gruner et al. only discloses that the single memory system can only be accessed by one of the plurality of processors at any one time.

Present claims 1 and 9, which have been amended to more clearly recite the invention, require that the memory module is divided into at least two banks wherein each bank can be accessed by more than one processor at any one time. Gruner et al., on the other hand, nowhere teaches or suggests that a plurality of processors can access a bank of the memory module or the module at any one time.

Furthermore, the memory module is mapped such that data at sequential addresses are stored in alternate banks. When a contention or memory conflict occurs, the processors are synchronized to access different blocks in the banks. Applicants submit that Gruner et al. also nowhere teaches or

suggests at least these limitations required by claims 1 and 9. Therefore, claims 1 and 9 are patentable over Gruner et al. Since claims 5-8 and 12-14 are dependent directly or indirectly on claim 1 or 9, these claims are also patentable over Gruner et al.

Rejection under 35 USC § 103(a)

Claim 12 is rejected under 35 USC § 103(a) as being unpatentable over Gruner et al. in view of US Patent 5,857,110 (Sakakibara et al.). Applicants respectfully disagree.

Applicants submit that there is no suggestion to combine Gruner et al. with Sakakibara et al. Even if there were suggestion to combine the references as suggested by the Examiner, this combination still fails to teach or suggest the invention of claim 12. Claim 12 is dependent on claim 9. As previously discussed with respect to the rejection to claim 9, Gruner et al. fails to teach or suggest at least accessing a memory module by more than one processor at any one time. Sakakibara et al., like Gruner et al., nowhere teaches or suggests accessing a memory module by more than one processor at any one time. Therefore, Applicants submit that claim 12 is patentable over Gruner et al. and Sakakibara et al., alone or in combination.

Independent claim 15 is rejected under 35 USC § 103(a) as being unpatentable over Gruner et al. in view of "The Cache Memory Book" (Handy). Applicants respectfully disagree.

Applicants submit that there is no suggestion to combine Gruner et al. with Handy. Even if there were a suggestion to combine the references as suggested by the Examiner, this combination still fails to teach or suggest the invention of claim 15. Claim 15, like claims 1 and 9, requires that the memory module is divided into at least two banks to enable the memory module to be accessed by more than one processor at any one time. In addition, claim 15 also requires that the memory module is mapped such that data at sequential addresses are stored in alternate banks and when a contention occurs, the processors are synchronized to access different banks. As previously discussed, Gruner et al. does not teach or suggest any of these limitations. The combination of Handy does not compensate for the defects of Gruner et al. since it only discussed the use of a cache memory. Therefore, claim 15 is patentable over Gruner et al. and Handy, alone or in combination. Since claims 18, 20-21 and 23-26

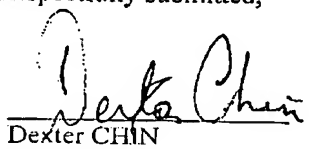
are directly or indirectly dependent on claim 15, these claims are patentable over Gruner et al. and Handy.

Conclusion

In view of the foregoing, it is respectfully submitted that all claims now pending in this application are in condition for allowance and the issuance of a formal Notice of Allowance at an early date is respectfully requested. Should the Examiner believe that a telephone conference would expedite prosecution of this application, please telephone the undersigned attorney at his number set out below.

Date: May 07, 2007

Respectfully submitted,



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